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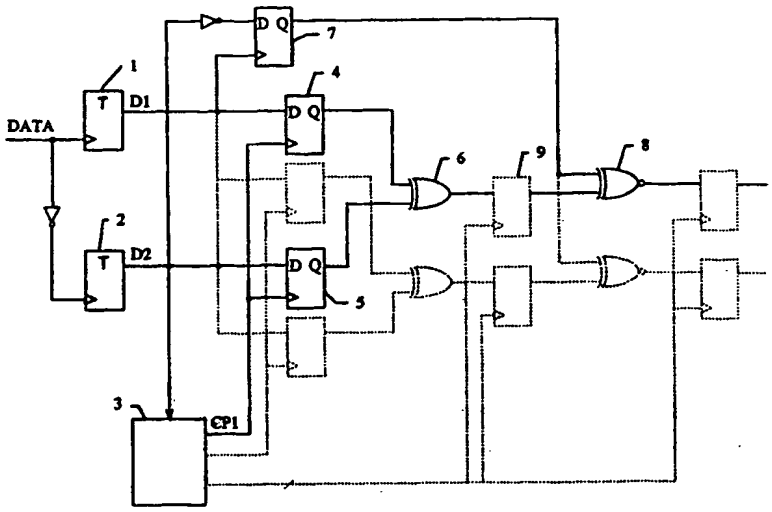
(54) Title: A METHOD OF GENERATING A PLURALITY OF DEMULTIPLEXED OUTPUT SIGNALS FROM A SERIAL DATA SIGNAL AND A CIRCUIT FOR PERFORMING THE METHOD



(57) Abstract

The invention relates to demultiplexing of high frequency data signals. The data signal is first frequency divided before extracting a clock signal, which is necessary to sample the data signal to provide plural, parallel data channels. The data signal is divided into two sub-signals (D1, D2) by means of toggle circuits (1, 2). On the basis of the sub-signal (D2), the circuit (3) generates a clock signal (CP1), which is used for sampling the sub-signals precisely at the time which causes transfer of information in the data signal to the respective channel. The output signal is generated via the XOR circuit (6), which recombines the sampled sub-signals, and finally the output signal is adjusted by means of the XNOR circuit (8) in accordance with the initial state of the sub-signals (D1, D2).

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A method of generating a plurality of demultiplexed output signals from a serial data signal and a circuit for performing the method

The invention relates to demultiplexing where a serial data flow with an associated high clock frequency is demultiplexed to a plurality of parallel channels.

Sampling of a data signal is based on a clock signal having a frequency which is twice as high as the frequency which represents the most rapidly occurring change in the logic signal levels of the data signal.

In connection with demultiplexing, the clock frequency may be reduced by a factor corresponding to the plurality of parallel channels, as the clock signals have a plurality of mutually shifted phases likewise corresponding to the plurality of channels. This is known from US Patent Specification No. 5 301 196, which also concerns generation of clock signals with a lower frequency than the data signal, a digital phase detector being used for controlling the clock generator.

Not only clock extraction, but also the subsequent sampling put a limit on how the bit rate on the serial input signal can be.

The object of the invention is to provide a method which, using a given electronic technology, enables demultiplexing of signals at a higher rate than has been possible till now with this technology.

This object is achieved by performing the method as stated in the characterizing portion of claim 1.

The invention is based on the circumstance that a simple division of the data signal may be provided at high frequencies, which are hereby divided to a level where also the sampling circuits are capable of coping. This allows working with such a high frequency on the serial data signal as makes it impossible in practice to sample directly on the data signal. Extraction of the clock signals from divided signals and sampling on the divided signals allow demultiplexing of data signals with considerably higher frequencies than has been possible in the past. The subsignals resulting from the division are finally combined, as stated in claim 1.

Preferably, two subsignals are provided, but these might also be divided again to provide four subsignals before the clock signal is extracted.

A preferred embodiment of the division of the data signal is stated in claim 3, and, as stated in claim 4, the clock signal is preferably generated from one of the subsignals.

Although the method operates at lower frequencies than the original data signal, the invention is preferably used at so high frequencies that signal processing after the sampling takes place in the vicinity of the upper limiting frequency of the circuits. It is therefore particularly important to provide alignment or synchronization of the parallel channels, and with this end in view additional phase shifted clock signals are generated to align the mutual temporal relation of the demultiplexed signals.

When the division of the data signal takes place e.g. as stated in claim 3, information is lost with respect to the initial state, i.e. whether the first switch in data

is from low to high or from high to low logic level. In connection with the combination of the subsignals to the demultiplexed output signals it is therefore necessary to add initial information which may be created from the subsignals.

The invention also relates to a circuit for generating demultiplexed output signals by performing the method of claim 1.

The circuit is characterized by the features defined in claim 6.

Typically, the frequency divider circuits comprise toggle circuits which are characterized by great simplicity and which are extremely fast.

As stated in claim 8, it is preferred to use XOR circuits for combining the demultiplexed subsignals.

The advantages of the invention are of quite special importance in connection with integrated circuits which consist of a large number of circuits having different logic functions. It is generally known that such different types of circuits in an integrated circuit have different maximum operating rates, and precisely the type of circuit which is known to operate most fast, e.g. toggles, may be used precisely for the operations requiring the high operating rate according to the invention, so that the circuits which operate relatively more slowly may be used particularly for the clock extraction.

The circuit of the invention can operate with data input signals which are so fast that they cannot propagate inside an integrated circuit. Although the circuit of the invention is used in connection with more moderate fre-

quencies of the data input signal, the invention provides the advantage that just a few very simple and fast circuits operate at a high frequency, while the other components in the integrated circuits may operate at reduced frequencies, thereby reducing the power consumption and heating of the circuit.

This ensures that an integrated circuit can operate at a signal input frequency which is at least twice as high as the signal frequency which the circuit is generally capable of handling.

The invention will be explained more fully by the following description with reference to the drawing, in which

fig. 1 shows a circuit for dividing the data frequency with a view to demultiplexing a serial data signal,

fig. 2 shows a circuit for demultiplexing a serial data signal,

fig. 3 shows the temporal course of selected signals in the circuit, and

fig. 4 shows the application of the invention in circuits of the ASIC type (Application Specific Integrated Circuit).

Fig. 1 shows a circuit for dividing the data frequency with a view to demultiplexing a serial data signal. The figure is simplified to clarify the description of the invention, so that parts important to the understanding are illustrated, while other parts are omitted or merely indicated.

The data signal DATA to be demultiplexed is fed to the frequency divider circuits 1 and 2. The number of frequency divider circuits depends on the selected embodiment, two being used in the preferred embodiment, and these are implemented using toggles. A toggle is a memory element having a clock input and a data output, the signal on the data output changing logic level each time the signal on the clock input switches from logic low to logic high level. A toggle is selected, because this is a relatively fast component allowing division of a high frequency data signal DATA, as described below.

As the data signal DATA is fed to the toggle 1 on its clock input, an output signal D1 will be generated, and this output signal changes logic level each time DATA switches from low to high logic level. The toggle 2 receives the inverted data signal on the clock input, and the output signal D2 will change logic level each time DATA switches from high to low logic level. The information from the data signal DATA is thus distributed on the signals D1 and D2, of which D1 contains information on the position of the logic switch from low to high level in the data signal DATA, and D2 correspondingly contains information on the position of the logic switch from high to low level. The generated signals D1 and D2 thus have a lower frequency, i.e. a lower information density, than the original data signal DATA. The average frequency of the signals D1 and D2 corresponds to one half of the average frequency of the signal DATA.

A plurality of clock signals having the same frequency and mutually different phases may be extracted from the signals D1 and D2. Thus, the clock signals are extracted from signals having a lower frequency than the data signal DATA, which allows a high data rate compared with the

use of prior art where the clock signal is extracted directly from the data signal DATA.

The preferred embodiment employs a clock extractor 3 which just uses the signal D2 for generating the clock signals. How the extraction takes place in detail is not described, as this forms no part of the invention, and as it is considered known to the skilled person how this is done in practice, e.g. using digital phase-locked circuits.

The generated clock signals are used for sampling the signals D1 and D2 by feeding the clock signals to the clock inputs of a plurality of sample-and-hold circuits. As illustrated in fig. 1, a D-flip-flop 4 is used as a sample-and-hold circuit, and this receives a clock signal CP1 on its clock input, said signal D1 being sampled when a clock pulse is received, said output being then held until the next clock pulse is received. The clock signal CP1 is likewise fed to a D-flip-flop 5, whereby the signal D2 is sampled and held.

The two sampled clock signals are fed to an XOR circuit 6, thereby combining the information from the two signals to one signal. The information from the data signal DATA is re-created hereby, but the initial information, i.e. whether the first switch in DATA is from low to high or from high to low logic level, is missing, because the initial state of the toggles 1 and 2 is unknown. This missing information, however, is added later in the circuit.

The output signal from the XOR circuit 6 is fed to a D-flip-flop 9 whose importance will be described in connection with fig. 2.

The information on the initial state is created using a D-flip-flop 7, the signal D1 being fed as a clock and the signal D2 being inverted and fed to the data input.

The start information signal and the output signal from a D-flip-flop 9 are fed to an XNOR circuit 8, whereby the signal receives initial information. The output signal from the XNOR circuit 8 is thus a signal containing information from the data signal DATA read at discrete times with a mutual temporal spacing corresponding to the cycle time of the clock signal CP1 and with an absolute position determined by the phase of the clock signal used.

Till now no demultiplexing proper has been performed, since this requires sampling using a plurality of clock signals with the same frequency, but with mutually different phases. As indicated by the dotted lines in fig. 1, the other clock signals from the clock extractor 3 may correspondingly be fed to a pair of D-flip-flops, so that the signals D1 and D2 are sampled at other times, depending on the phase of the clock signal. How the individual clock signals are phase-shifted with respect to each other, and how the signals D1 and D2 are sampled hereby, will be described more fully in connection with fig. 2.

In the simplified embodiment illustrated in fig. 1, the various output signals will be mutually phase-shifted because of the phase difference between the clock signals which were used in the corresponding samplings of the signals D1 and D2. Fig. 2 shows in greater detail how the invention may be implemented and gives an example of how the phase difference between the demultiplexed signals may be corrected.

Fig. 2 shows an example of how the circuit of fig. 1 may be incorporated in a circuit for demultiplexing a serial data signal to two output signals. The parts in the figure which are the same as those in fig. 1 have identical reference numerals.

The data signal DATA is fed to the toggle 1 and is inverted and fed to the toggle 2, whereby it is divided to the signals D1 and D2.

The signal D2 is fed to the clock extraction circuit 3 which extracts a plurality of clock signals with the same frequency, but with mutually different phases. The frequency of the clock signal corresponds to one half of the frequency which is to be used as a basis in the sampling of the data signal DATA. The clock signal CP1 is fed to the D-flip-flops 4 and 5, whereby D1 and D2, respectively, are sampled. Correspondingly, the clock signal CP2 is fed to D-flip-flops 10 and 11, which also sample the signals D1 and D2. An expedient selection of phase difference between the clock signals CP1 and CP2 will cause sampling of the data signals so that the sample values may be used for generating the demultiplexed data signals. This is illustrated in fig. 3. In addition to the said clock signals CP1 and CP2, the clock extraction circuit 3 moreover extracts a plurality of clock signals CP3. These will be described more fully below.

The sampled signals are fed to the XOR circuits 6 and 12, whereby the information created corresponds to the information in the data signal DATA, apart from the missing information on the initial state.

The output signals from the XOR circuits 6 and 12 are phase-shifted corresponding to the phase difference between the clock signals CP1 and CP2. TO reduce the phase

difference between the two generated signals, D-flip-flops 9 and 13 are inserted, said D-flip-flops 9 and 13 using clock signals CP3 from the clock extractor 3 as clock signals. Expedient selection of the phases of these fed clock signals CP3 may result in a reduction of the phase difference between the data signals.

The output signals from the D-flip-flops 9 and 13 are combined with the initial information from the D-flip-flop 7, and the demultiplexed output signals are generated by utilizing the XNOR circuits 8 and 14.

A final alignment of the phase is made, as illustrated, with D-flip-flops 15 and 16 by clocking these in phase. The phase alignment is performed in several steps because a joint phase alignment using a single D-flip-flop makes relatively great requirements with respect to the speed of the flip-flip circuit owing to the small setup times. In contrast, an expedient division allows longer setup times and is therefore less exacting with respect to the speed of the flip-flop circuit. Another reason why it is expedient to split the phase alignment is that this allows the relatively slow XOR and XNOR circuits to be positioned between the D-flip-flop circuits.

Fig. 3 shows an example of the course of selected signals in fig. 2 when the data signal DATA is fed to the circuit. For clarity, the phase alignment, considered well-known to the skilled person, is disregarded. As the figure does not illustrate the phase alignment, the demultiplexed output signals X3 and X4 are phase-shifted in fig. 3, corresponding to the phase-difference between the clock signals CP1 and CP2.

The temporal course of a selected data signal DATA is shown at the top of the figure. Fig. 3 also shows the

temporal course of the subsignals D1 and D2 which are generated from the data signal DATA using a pair of toggle circuits, as shown in fig. 2.

Next are the extracted clock signals CP1 and CP2, which have the same frequency, but different phases. The signal S1 and S2 is generated by sampling the signal D1 using the clock signal CP1 and the clock signal CP2, respectively. S3 and S4 is generated correspondingly by sampling the subsignal by sampling of the signal D2 with the clock signal CP1 and the clock signal CP2, respectively.

The signal X1 is formed from the signals S1 and S3 by performing an XOR function. Correspondingly, the signal X2 is formed by performing an XOR function of the signals S2 and S4.

The start information signal START is formed from the signals D1 and D2 and has the logic value zero in this case. The output signals X3 and X4 are generated by combining X1 and X2, respectively, with the initial information START, using an XNOR function. As appears from the figure, the demultiplexed output signals X3 and X4 contain the information from the data signal DATA, and demultiplexing of the signal DATA, i.e. 0101101001, by demultiplexing to two output signals is expected to result in the signals 00110 and 11001, which are found in the signals X4 and X3.

Fig. 4 symbolizes an integrated circuit of the ASIC type (Application Specific Integrated Circuit), which is generally designed by the reference numeral 40. Such a circuit contains a very large amount of components (i.a. symbolized by the non-numbered areas), and the invention also relates to a layout of such a circuit for performing the method. Toggle circuits are shown at 41 and 42,

adapted to divide the input signal DATA IN, said circuits being connected to other circuits such as 43-46, whose function may be compared with the disclosure in connection with fig. 1. The circuit 40 may hereby be used in connection with data input signals whose frequency is so high that the clock extractor 43 usually cannot cope, and the frequency of the data input signal may moreover be so high that it is impossible in practice to feed the signal and e.g. sample directly on it inside the circuit. Therefore, the toggles 41 and 42 are preferably arranged in the vicinity of the outer rim of the circuit 40.

Although a preferred embodiment of the present invention has been described and shown, the invention is not limited to it, but may also be embodied in other ways within the scope of the subject-matter defined in the appended claims.

Patent Claims:

1. A method of generating a plurality of demultiplexed output signals from a serial data signal, comprising

splitting the data signal into at least two subsignals which have a lower information density than the data signal, and

extracting mutually phase-shifted clock signals from the split subsignals,

characterized by

using the clock signals for sampling the subsignals to generate a set of demultiplexed subsignals, and

combining the demultiplexed subsignals to form the demultiplexed output signals.

2. A method according to claim 1, characterized by splitting the data signal into two subsignals.

3. A method according to claim 1 or 2, characterized by performing the frequency division such that one divided signal changes logic level each time the data signal switches from low to high logic level, while the other frequency-divided signal changes logic level each time the data signal switches from high to low logic level.

4. A method according to claims 1 to 3, characterized by generating the clock signal from one of the subsignals.

5. A method according to any one of the preceding claims, c h a r a c t e r i z e d by generating additional mutually phase-shifted clock signals, and using these to achieve synchronization of the demultiplexed output signals.

6. A circuit for generating a plurality of demultiplexed output signals from a serial data signal, said circuit comprising

frequency divider circuits adapted to generate, from the data signal, at least two subsignals which have a lower information density than the data signal, and

extraction circuits adapted to generate mutually phase-shifted clock signals from the split data signals,

c h a r a c t e r i z e d by

a plurality of sampling circuits adapted to sample the subsignals in accordance with the mutually phase-shifted clock signals to generate a set of demultiplexed subsignals, and

a combination circuit adapted to receive the demultiplexed subsignals and to generate the demultiplexed output signals.

7. A circuit according to claim 6, c h a r a c t e r - i z e d in that the frequency divider circuits comprise toggle circuits.

8. A circuit according to claim 6, c h a r a c t e r -

i z e d in that the combination circuit comprises an XOR circuit whose input terminals are connected to receive a respective one of the demultiplexed subsignals.

9. An integrated circuit for digital signal processing comprising demultiplexing a serial data signal, said circuit comprising two or more types of circuits, one type being relatively fast, the other types being relatively slower circuits, c h a r a c t e r i z e d by including

two or more frequency dividers adapt to frequency-divide the data signal,

a clock extractor adapted to receive the frequency-divided data signal and to generate clock signals having mutually different phases,

sampling circuits adapted to sample the frequency-divided signals in response to the mutual phase-shifted clock signals to generate a plurality of demultiplexed subsignals,

a combination circuit adapted to receive the demultiplexed subsignals to generate a demultiplexed representation of the serial data signal, and

that the circuits for frequency division are selected from the relatively fast type of circuits in the integrated circuit, while the other circuits are preferably selected from the relatively slower circuits in the integrated circuit.

10. A circuit according to claim 9, c h a r a c t e r i z e d in that the circuits for frequency division are toggle circuits.

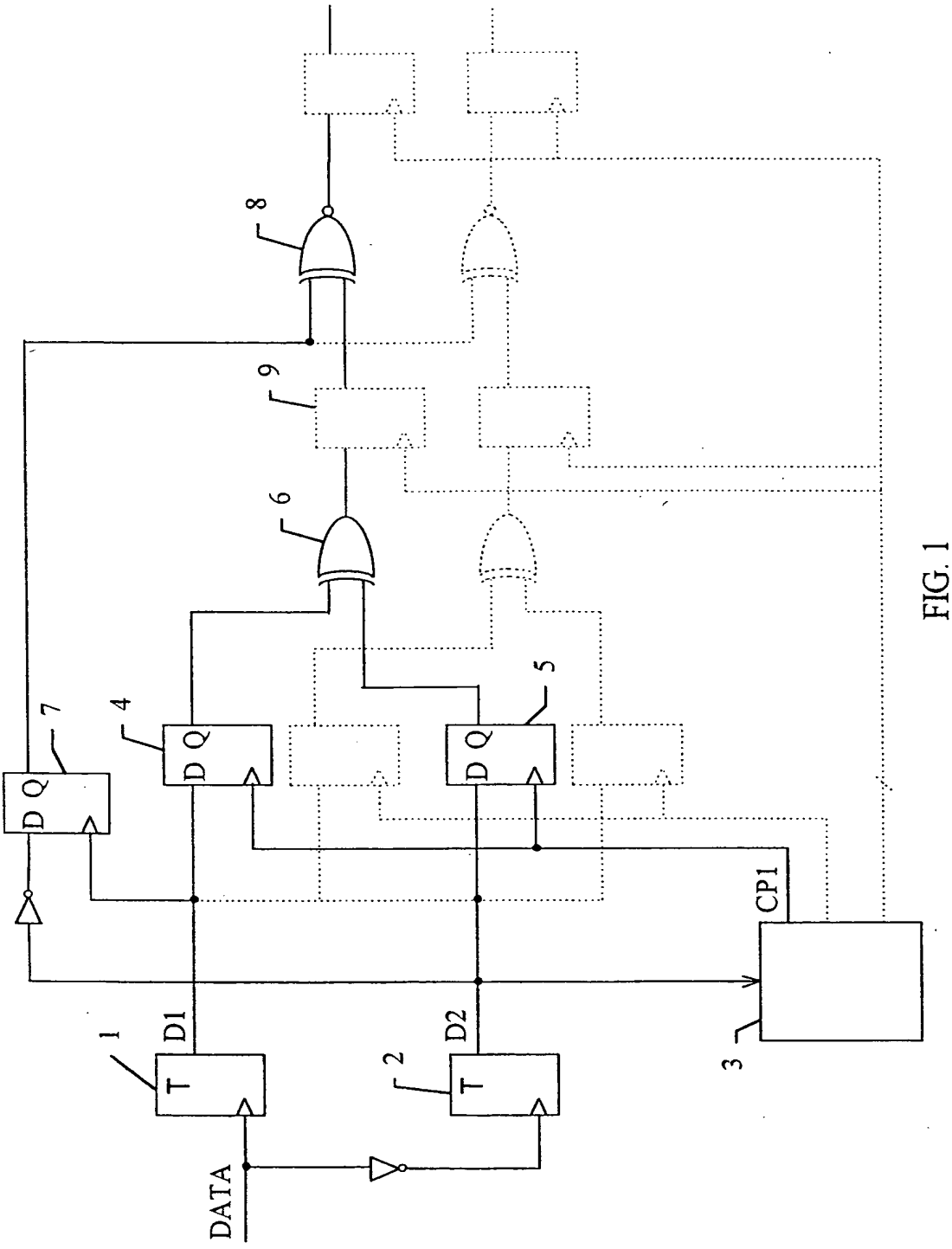
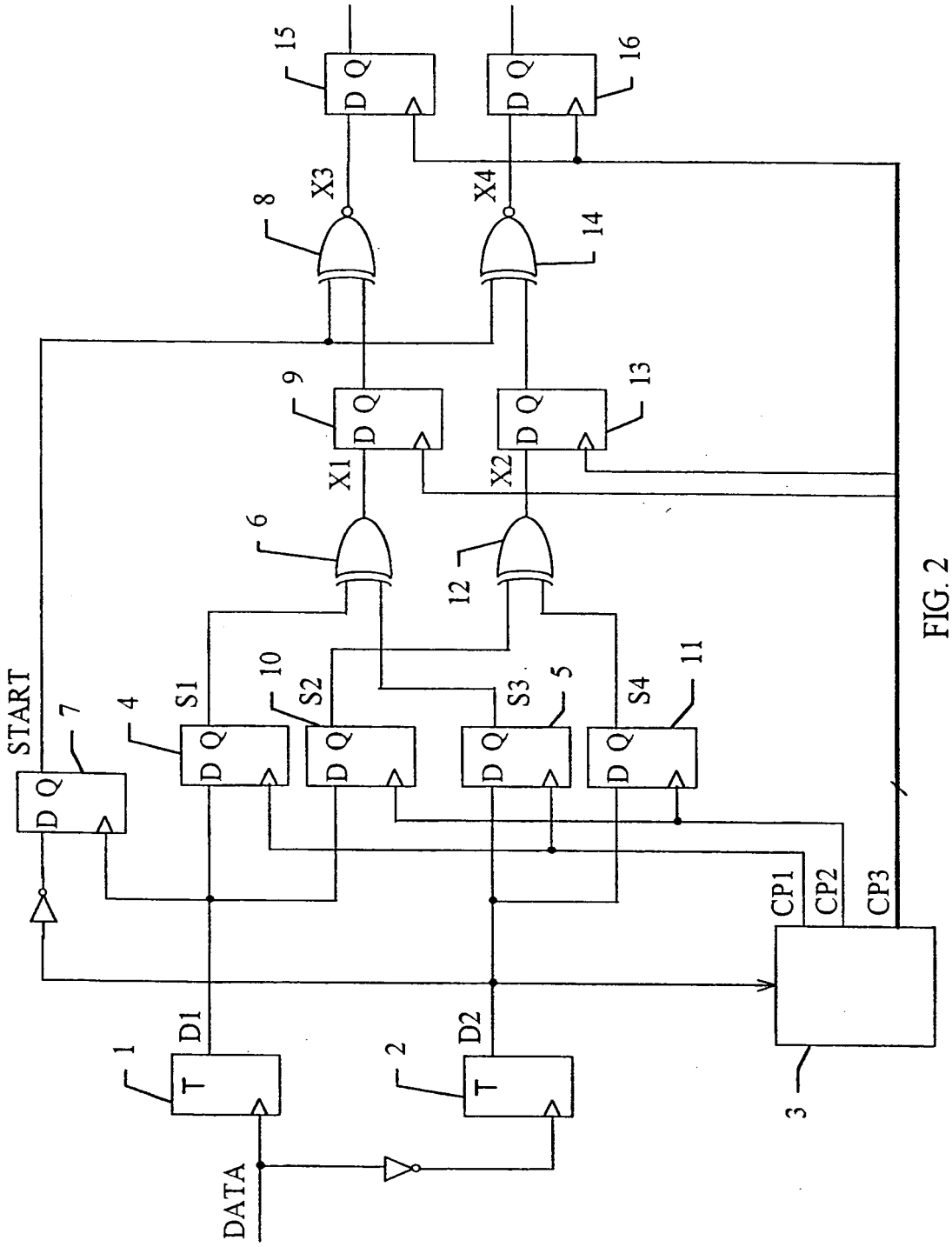


FIG. 1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16
X3
X4
8
14
9
13
X1
X2
6
12
START
7
4
S1
10
S2
S3
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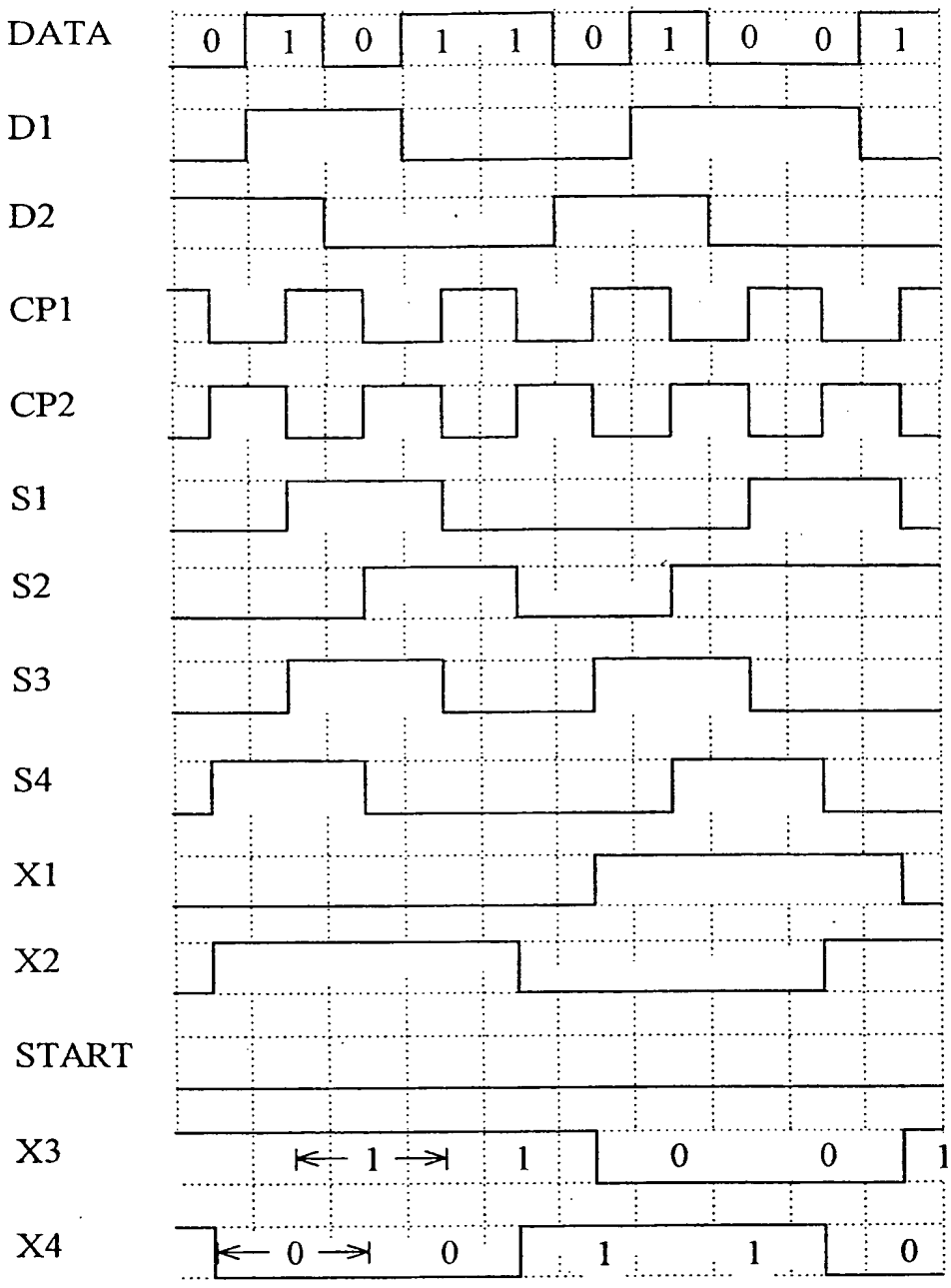
S4
11
CP1
CP2
CP3
D1
D2
1
2
3
DATA
D Q
T

FIG. 2


DATA
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D1
D2
CP1
CP2
S1
S2
S3
S4
X1
X2
START
X3
1 1 0 0 1
X4
0 0 1 1 0

FIG. 3

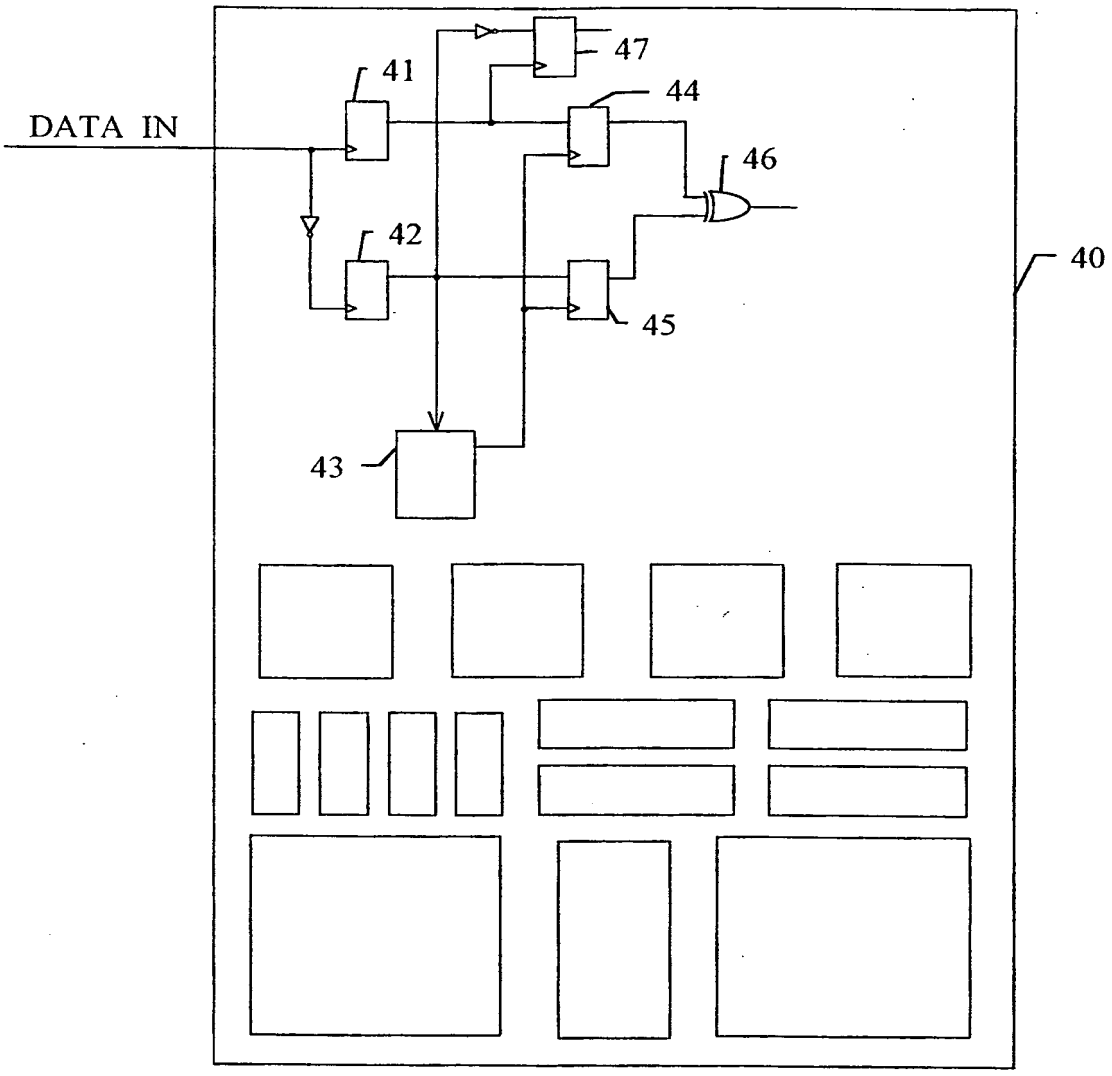

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 97/00579

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04J 3/04, H04L 25/02 // H04L 7/033
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5301196 A (JOHN F. EWEN ET AL), 5 April 1994 (05.04.94), column 1, line 6 - line 12; column 3, line 42 - column 4, line 15; column 4, line 51 - column 5, line 10, figures 1,2A --	1-10
A	DE 3640874 A1 (SIEMENS AG), 9 June 1988 (09.06.88), figure 2, abstract --	1-10
A	DE 4410552 A1 (LAO,ZHIHAO), 5 October 1995 (05.10.95), figures 1,5, abstract --	1-10
A	US 5128940 A (HIROTSUGO WAKIMOTO), 7 July 1992 (07.07.92), figure 4, abstract --	1-10

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 May 1998	13 -05- 1998
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Anders Ströbeck Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 97/00579

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

Information on patent family members

29/04/98

International application No.
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